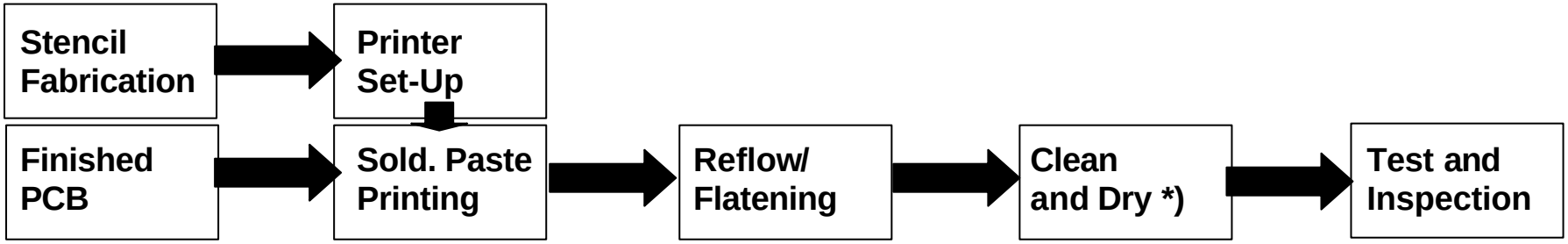
Solid Solder Deposit SSD - New Interconnection Technology

Technology Supplier Mask Tek Santa Ana
Plating Technology

Project Team: MaskTek, Siemens A&D, Siemens CT
Assy Tests 11/98 to 2/01

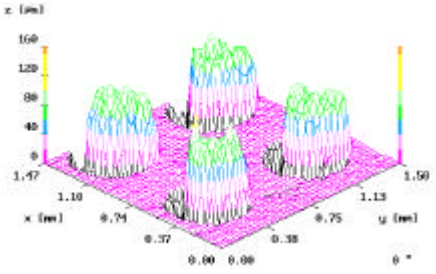
SSD - Process Flow

The SSD process is comprised of the following;
1) Solder paste print using conventional methods;
2) Reflow/formation of the deposits using equipment licensed specifically for this purpose;
3) Cleaning in the event that a water soluble paste is employed.



The PPT Process Flow Chart, ***)** (if necessary)

Solder Paste:
Conventionell SnPb62(Ag) and Sn43Pb43Bi14, Sn95-96.5Ag3.5-5, SnAg3.8Cu0.7
(water soluble and/or no-clean, powder type 3), modified mediums
Solder Paste Thickness (100 to 120 µm)



SSD- Heigth

Board Parameters
Laminates FR 4, Polyimid, Teflon, Ceramic, Flex and Wafer
Board-Finishes: HAL, Ni-Au, immersion Sn, Cu OSP
Pad-Ø: Shielding frames up to 0.3 - 0.1 mm (Area Array)

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Print Parameters

40 psi pressure, blades metal blade with Permalex Coating, angle 40-45°
(wet thickness is not measured)
Stencil (Material stainless steel, laser cutted, electropolished, thickness (100 to 120) µm, aperture 1 : 1)
SSD Thickness 0,0005'' to 0.040'' (TAB package to mechanical connectors)
Tolerancies Solder Paste Thickness (0.0025'' - SSD thickness +/-0.0002 - 0.0003'')

PPT Reflow Equipment - Reflow Process

Subsequent to paste print panels or arrays are loaded into the patented PPT™ Reflow Equipment.
A tensioned stainless steel mesh is lowered onto the panels or arrays and a hot air knife travels over the boards.
The traveling heat source is designed to insure a very brief thermal excursion (Table 1).
While solder paste manufacturers normally recommend a reflow stage of 30-90 seconds for eutectic solder at a temperature of 180-235°C, in the SSD process time at temperature is normally less than 20 seconds.
The flux carrier used in the paste and the absence of components during solder formation both facilitiate rapid reflow.
The mesh used in the SSD process acts as a die or mold to flatten (planarize), shape and remove excess solder during reflow. Alternatively, solder spheres (or bumps in wafer bumping) can be formed with the mesh screen acting as a conduit for excess solder to rise and be removed.

The mesh controls solder in the Z axis and enables volatiles present in the solder paste to escape during reflow and SSD formation which occur simultaneously. Excess solder wicks above the mesh during reflow in the form of solder balls. The reflowed solder deposits are macro-planar with an embossed surface topography that retains a high volume of tack flux at subsequent assembly. Further this conduit, created by the mesh, enables the solder to be formed without voids.

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Common SSD Reflow Profile - Sn63/Pb37

Peak Temperature	214.5°C
Time over 150°C	57.5 Seconds
Time over 180°C	15.0 Seconds
Time over 200°C	6.0 Seconds
Time over 210°C	2.5 Seconds

SSD "flat pad" on .020" pitch SMD

After reflow solder deposits are quenched with a lower temperature cooling pass and boards exit the system.

Cleaning Items, Frequencies

Only when water soluble pastes were applied

Process Discription

Mesh - (diameter 40 µm - conventional pad constructions, 28 µm for FC),
Mesh-Construction (mesh count conventional package 200 / sqinch; FC 325 / sqinch), open area 48 % / 39 %FC
The wire-mesh screen process provides a very defined volume of solder which cannot be accomplished with normal stencil printing. Shorts and solder balls at assembly are eliminated and the copper lands are encapsulated in a thick solder deposit which increases bare board shelf life.

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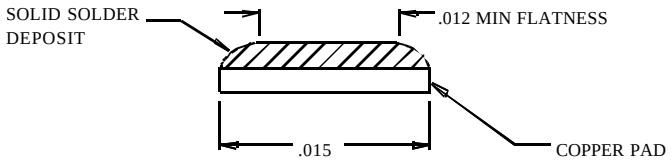
SSD Thickness/Uniformity - Conventional SMD

	Range	Uniformity
BGA	.0019-.0025”	+/- .0003”
PLCC	.0019-.0029”	+/- .0002”
QFP	.0019-.0024”	+/- .0002”
SOIC	.0019-.0029”	+/- .0002”
TSOP	.0010-.0022”	+/- .0002”

Solder Deposit Planarity/Sphericity

Planarity specifications vary due to a number of criteria including board design, land configurations, pitch, buried vias in the pads or vias connected to the pads which can effect solder volume as well as alloy. Further it is common for the deposits to have a ”shoulder” as depicted in the drawing below. A planarity specification of .012” minimum flatness, or 80% of the surface area, allowed for up to +/- .006” of leg misalignment in the lateral direction for one end user. For another manufacturer of memory modules first pass yields on µBGA devices increased from 64% to 99.7%.



Inspection Technology of Paste Printing Not Required

Responsibility of PCB supplier

SSD Process Flow

SSD and Assembly Process Discription

Bare Board

SSD application (see attached discription)

Adhesion and Wetting Promoter
Variables (Dispensing, Jetting, Pin Transfer, Spraying, Tape)

Adhesion and wetting promoter on SSD top, stackable
(PSA - Pressure sensitive adhesive,
placement forces)

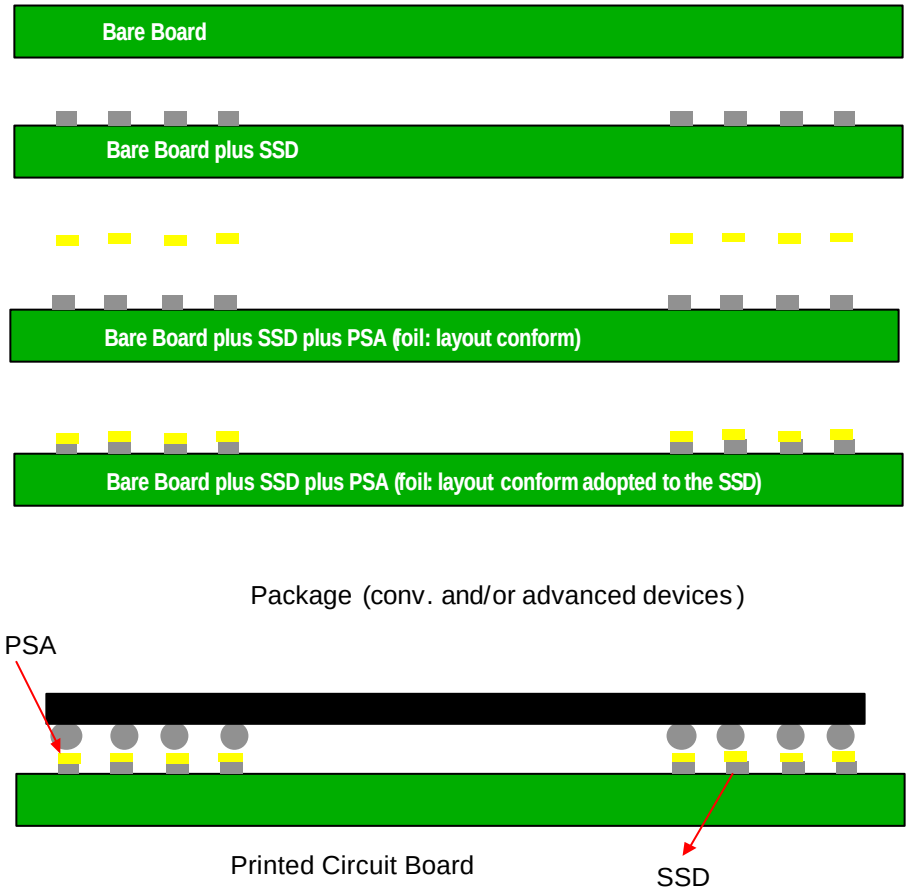
Placement - SSD - Package-Tolerancies

Reflow (conventional parameters)
Yield (must be compared to conventional packages)

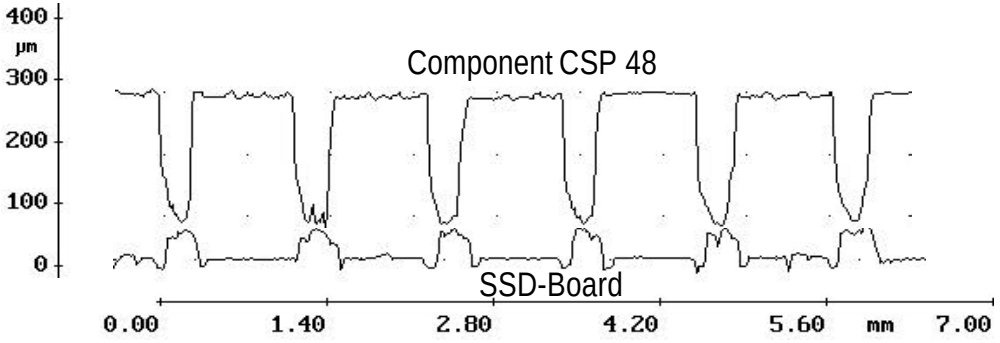
Microsection (interface characterization)

Board Level Reliability

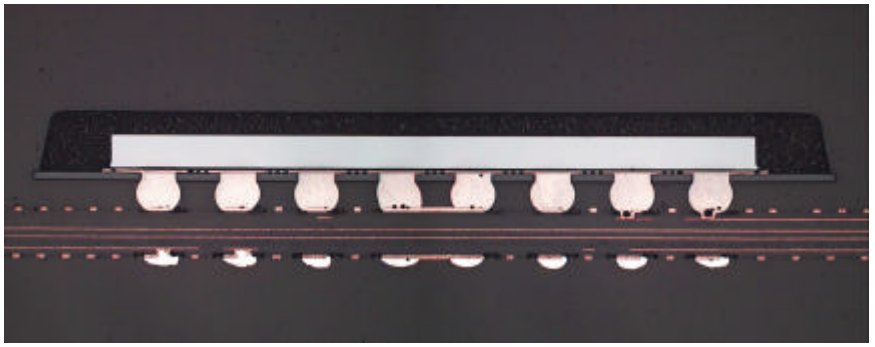
Process Flow SSD PSA Preplated PCB



Assembly Results



Coplanarity Result for CSP Packages



Microsection after SSD + CSP - Reflow

Test Data

First pass yield and assembly troughput
Assembly tests done for single and double sided boards (PCMCIA card, Simatic boards), adhesion promoter transfer by flux dipping CR 32 (75 to 185 µm)
Reflow under normal and nitrogen atmosphere, Peak-temperatures 230 °C with Pb-free SSD topologies

Costs

Comparison to Ni-Au, imm. Sn

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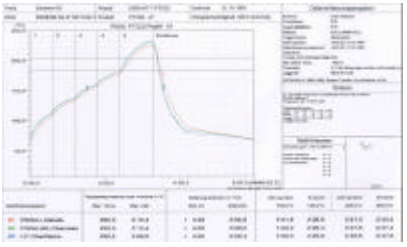
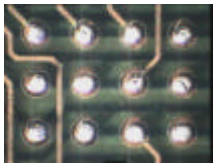
Summary SSD Testboards and Assembly-Parameters

PCB plus SSD

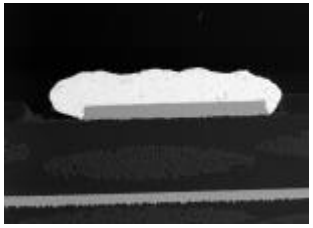
Flux Dipping

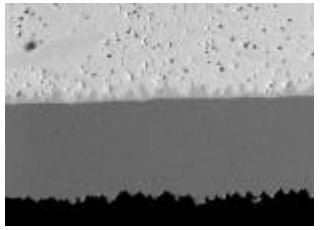
- **No Solder Paste Printing in Assy Line**
- **Adhesion / Wetting Support**
- **Determine automatic placement parameters on Siplace 80F^5**
- **Conventional Reflow Profile (SnPb or Pb-free Solders), Peak 230 °C**
- **SSD inspection by transmission x-ray and cross sections**





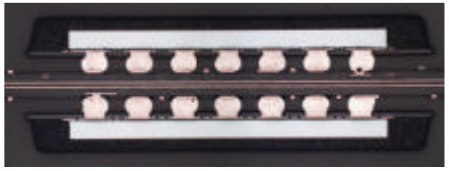
SSD depot after PPT process

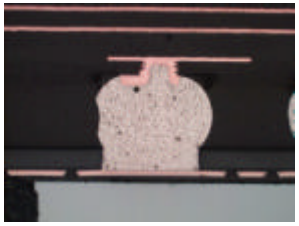




Interface analysis - SnAgCu deposit

Single sided assembly - CSP





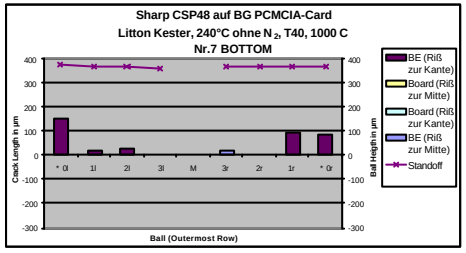
Double sided assembly - CSP

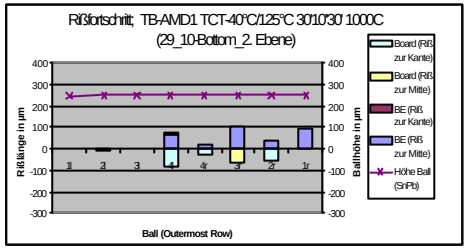
Summary SSD-Testboard - Acceptance Criterias

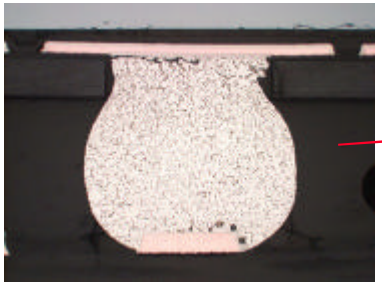
Assembly overview

Comparison of Crack Length: Left CSP on SSD-preplated, boards; Rigth: CSP on Ni-Au

Note: Interface stability in case of SSC, no cracks at PCB Side







2nd level reliability tests

- **TCT40** TCT -40/+125°C (30'10''30')
- **TCT20** TCT -20/+100°C (30'10''30')
- **THB** Thermal humditiy 85°C/85%

Comparison BLR Results SSD on PCMCIA Testboard with Area Array Packages

Will be completed

Conclusions / Acceptance criterias

- **Lifetime-comparison with other board finishes ...)**
- **Higher interface stability related to conventional finishes**
- **N_0, $N_{0.1}$, N_{63} vs. b-comparison necessary**